Yin Fung Khong

yinfung96@gmail.com | (206) 434-2327 | yinfung96.github.io | linkedin.com/in/yinfungkhong

A M.S. in Computer Engineering diverse set of engineering skills in hardware and software design to project management. Equipped with research publications experience developing MATLAB algorithm involving image processing and internship experience at Intel developing software automation tool for hardware test data analysis using C#. Proficient in hardware RTL coding and low-level programming such as Verilog and ARM. Strong communication skill working in diverse teams.

FPGA/ASIC Design| RTL Design Implementation | Software Programming | Project Management | Research Publication | Problem Solving | Self-Motivated | Analytical Thinking | Attention to Detail | Communicator | Team-Player

EDUCATION

Master of Science (M.S.) in Computer Engineering, 2019, GPA 3.94/4.0
Bachelor of Science (B.S.) in Computer Engineering, 2018, GPA 3.94/4.0
California State University, Northridge (CSUN)

- **Awards:** Outstanding Graduate Student, Summa Cum Laude, Distinction Award, Dean's List
- **Coursework:** Digital Systems Design with Programmable Logic, System on a Chip (SoC) Design, Digital Design with Verilog and System Verilog, FPGA/ASIC Design and Optimization using VHDL, Microprocessor Systems, Diagnosis and Reliable Design of Digital Systems, Digital System Design Automation and VHSL Modeling

RESEARCH PUBLICATION

S. Semerjian, Y.F. Khong, S. Mirzaei, **White Blood Cells Classification using Built-In Customizable Trained CNN,** *IEEE International Conference on Systems, Man, and Cybernetics 2020*, Toronto, Canada. Apr 2020. Submitted.

Y.F. Khong and S. Mirzaei, **A Novel Approach for Efficient Implementation of Nucleus Detection and Segmentation Using Correlated Dual Color Space**, *IEEE International Conference on Systems, Man, and Cybernetics*, Oct 2019.

SKILLS

Programming: Verilog, System Verilog, VHDL, ARM Assembly, MATLAB, Python, VBA, C, C#, AHK, Java, HTML
Tools: Xilinx Vivado HLS, Xilinx Zedboard, Cadence SPICE, Synopsys, VCS, JMP, Laboratory Equipment, LPC2148

PROJECTS

RTL RISC-Y Processor using Verilog and System Verilog

- Designed and implemented synthesizable RTL design of a RISC-Y processor that has immediate or direct addressing mode by modules such as scalable MUXs, sequence controller, scalable register files, AASD and ALU.
- Created System Verilog simulation testbenches to verify proper design functionalities and to debug the module.
- Authored documentations of the project in detail with a slideshow presentation of the design and result.

RTL FPGA Multi-Clock and Timers using Zedboard SoC Development Board

- Designed and implemented high performance RTL chess clocks and countdown timers targeting FPGA in VHDL.
- Designed and debugged the RTL design consists of FSM for state handling, LFSR for pseudo-random number generation and clock divider. Performed hardware simulation and functional verifications of the design.

Automated Music Box using Xilinx FPGA Zedboard and MATLAB Image Processing

- Implemented the Optical Recognition System using MATLAB to extract the musical data such as frequency and duration of the note from a camera image, which they will be stored into an SD memory card.
- Configured SDIO to read the data and store them into the on-board BRAM which will further process via software implementation to allow music playback via a connected speaker.

EXPERIENCE

Software Optimization Engineer & Project Manager Team Lead

ISI Language Solutions ***09/2019 – present***

- Interacts with internal software team and production team to understand design requirements and opportunities to optimize production workflow by creating and implementing various software automation tools.
- Designs and debugs software automation tools for the production team, saving production labor and cost by 60%.
- Interacts with external vendors to communicate projects requirements while ensuring project's progress.
- Creates and presents detailed reports of progress and applicable metrics to Production Managers, ensuring efficient coordination and utilization of resources and tools while meeting 100% of projects deadlines.

Graduate Research Assistant

CSUN Dept of Electrical & Computer Engineering ***08/2018 – 07/2020***

- Researched two efficient algorithms for nucleus segmentation and classifications of blood cells in microscopic blood images using digital image processing techniques to accelerate and improve accuracy in blood diagnosis.
- Developed a highly versatile image processing technique to segment nuclei from a broad spectrum of blood images while retaining cell features and integrity in the processed image up to a 98.99% accuracy using MATLAB.

Graduate Assistant

CSUN Dept of Electrical & Computer Engineering ***08/2018 – 05/2019***

- Led in weekly lab sessions, provided valuable inputs, suggestions and guidance to students in safe operations of laboratory optical and electrical characterization tools such as logic analyzers and DMMs.
- Assisted approximately 200 students by grading and providing feedback to students based on their performance.

Hardware Verification - Graduate Intern

Intel Corportation ***06/2018 – 08/2018***

- Performed detailed analysis on the existing data analysis workflow, communicated applicable metrics and specifications of the automation tool, and proposed the overall idea to the entire team for feedback.
- Developed and debugged a C# automation tool to automate statistical test data analysis using output data from an Automated Test Equipment (ATE), increasing the team's efficiency by 65%.

LEADERSHIP

Co-founder and Student Coordinator

College of Engineering and Computer Science Mentorship Program ***01/2020 / 05/2019***

- Spearheaded and piloted the mentorship program within 2 months to improve students learning outcomes within the college by offering peer-to-peer mentorship and referral of resources to the student.
- Recruited and managed a team of 10 student mentors to develop and coordinated program events with the Dean's Office and Student Services to address common challenges faced by students.

President

Tau Beta Pi Engineering Honor Society ***06/2017 – 05/2019***

- Re-chartered the chapter in the college, initiated over 140 active members while leading a 19-person leadership team. Reported to 5 faculty advisors in the organization weekly to update and propose new ideas for approval.
- Maintained industrial connections, coordinated over a total of 30 professional development workshops and networking events on campus, benefiting over 300 member and non-member engineering students in the college.
- Awarded "Best Leadership Award" and "Effective Use of Technology" in adopting changes to positively impact chapter's membership and engagement.